(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 March 2002 (07.03.2002)

PCT

(10) International Publication Number
WO 02/19050 A1

(51) International Patent Classification[7]: G05F 3/26

(21) International Application Number: PCT/EP01/10110

(22) International Filing Date: 29 August 2001 (29.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
00203033.6 1 September 2000 (01.09.2000) EP

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: VOORMAN, Johannes, O.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). DE JONG, Gerben, W.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). WAFFAOUI EL, Rachid; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: DE JONG, Durk, J.; Internationaal Octrooibureau B.V., Prof Holstlaan 6, NL-5656 AA Eindhoven (NL).

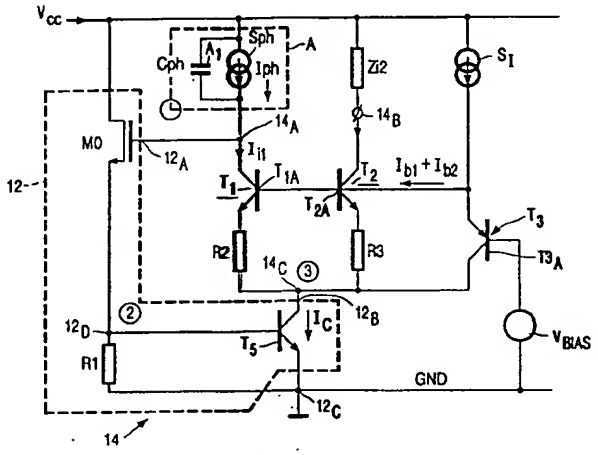
(81) Designated States *(national)*: CN, JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CURRENT MIRROR CIRCUIT



(57) Abstract: A current mirror circuit is described which includes a current input terminal (14A), a current output terminal (14B) and a common terminal (14C). A first controllable semiconductor element (T1) is arranged between the current input terminal (14A) and the common terminal (14C). A second controllable semiconductor element (T2) is arranged between the current output terminal (14B) and the common terminal (14C). The controllable semiconductor elements (T1, T2) havie interconnected control electrodes (T1A, T2A) which are also coupled to a bias voltage source (VBIAS), for biasing said control electrodes at a reference voltage. The circuit further includes a transconductance stage (12) with an input (12A) coupled to the current input terminal (14A) and an output (12B) coupled to the common terminal (14C). The control electrodes (T1A, T2A) are coupled to the common terminal (14C) via a third controllable semiconductor element (T3). The bias voltage source (VBIAS) is coupled to the control electrodes of the first and the second controllable semiconductor element (T1, T2) via a control electrode (T3A) of the third controllable semiconductor element (T3). The current mirror circuit has a high bandwidth also at low input currents and is very suitable for application in an arrangement for reproducing an optical record carrier.

WO 02/19050 A1

Current mirror circuit

The invention pertains to a current mirror circuit including a current input terminal, a current output terminal and a common terminal, a first controllable semiconductor element arranged between the current input terminal and the common terminal, a second controllable semiconductor element arranged between the current output terminal and the common terminal, the controllable semiconductor elements having interconnected control electrodes which are also coupled to a bias voltage source, for biasing said control electrodes at a reference voltage, the circuit further including a transconductance stage having an input coupled to the current input terminal and an output coupled to the common terminal.

Such a current mirror circuit is known from WO 00/31604. In the known circuit the transconductance stage generates a current which is divided over the first and the second semiconductor element, so that the input voltage is maintained close to a reference voltage. It is realised therewith that the input impedance is significantly decreased so that a large bandwidth is obtained. However, in the known circuit the imput impedance depends relatively strongly on the current amplification factor of the first and second controllable semiconductor elements, which on its turn is dependent on the input current. As the source of the input current generally has a finite impedance, this entails that the bandwidth of the mirror circuit is dependent on the input current.

It is an object of the invention to provide a current mirror circuit according to the opening paragraph in which the depence of the bandwidth on the input current is reduced. According to the invention the current mirror circuit is characterized in that the control electrodes are coupled to the common terminal via a third controllable semiconductor element, and in that the bias voltage source is coupled to the control electrodes of the first and the second controllable semiconductor element via a control electrode of the third controllable semiconductor element. At a low input current the current amplification factor of the first and the second controllable semiconductor element strongly reduces. This has the

effect that a relatively large current flows via the control electrodes of these semiconductor elements. In the current mirror circuit of the invention the current via the control electrodes to the common terminal flows back via the third controllable semiconductor element, so that this effect is compensated. As a result the imput impedance, and therewith the bandwidth is less dependent on the input current.

In a preferrable embodiment the interconnected control electrodes are further connected to a current source. This current source may serve at the same time to bias the third semiconductor element and to bias a component of the transconductance stage.

A further preferable embodiment is characterized in that the first and the second semiconductor elements have an area ratio 1:P. In that way the circuit operates as a current amplifier.

A still further preferable embodiment is characterized in that the first and the second semiconductor elements are bridged by a first and a second capacitive impedances having a capacitive value with a ratio of 1 to P. This measure further improves the bandwidth. The high frequency components generated by the transconductance stage are divided over the first and the second capacitive impedances in a ratio determined by the ratios of their capacitive values. As the ratios of the capacitive values corresponds to the area ratios of the controllable semiconductor elements a flat amplification-frequency characteristic is obtained over a large frequency range.

Another preferable embodiment of the invention is characterized in that the interconnected control electrodes are further connected via a third capacitive impedance and via a fourth controllable semiconductor element to a reference voltage, and that a control electrode of the fourth controllable semiconductor element is coupled to the common terminal. In the circuit of the invention the common terminal shows relatively large voltage variations. These may induce losses via stray capacitances. The auxiliary circuit formed by the third capacitive element and the fourth controllable semiconductor element achieves that these losses are compensated for, as a result of which the bandwidth is still further improved.

An integrated circuit according to the invention comprises at least one current mirror circuit according to the invention, and a photodiode having an output coupled to its current input terminal. The integrated photodiodes have a relatively small capacitance as compared to discrete photo diodes, which is also favorable for the bandwidth.

Such an integrated circuit is described in more detail in the ANNEX: "High-Bandwidth Low-Capacitance Integrated Photo Diodes for Optical Storage".

Figure 1 schematically shows an integrated circuit comprising photodiodes A,...,F. The photodiodes A,....,D are coupled to current pre-amplifiers 1A,...,1D and the photodiodes F and G are coupled to transimpedance amplifiers 3F and 3G respectively. The current pre-amplifiers 1A,...1D each have a first output coupled to a respective transimpedance amplifier 2A,...,2D. The current pre-amplifiers 1A,...1D each have a second output. The latter are interconnected as well as connected to the input of a further transimpedance amplifier.

One of the current pre-amplifiers is shown in more detail in Figure 2. The current amplifier comprises a cascade of current mirrors 14, 18, 22 and 26. to amplify the signal provided by the diode A. The current amplifier comprises a current mirror circuit 14 including a current input terminal 14A coupled to the photo diode A, a current output terminal 14B and a common terminal 14C. A transconductance stage 12 has an input 12A coupled to the current input terminal 14A and an output 12B coupled to the common terminal 14C. The transconductance stage has a further input 12C coupled to a reference voltage source 10. Likewise current mirror circuits 18 and 22 are coupled to a transconductance stage 16 and 20. Also the current mirror circuit 26 is coupled to a transconductance stage 24, but in this case the output of the transconductance stage 24 is coupled to the mutually interconnected control electrodes of the controllable semiconductor elements 26A, 26B forming part of this current mirror circuit.

Figure 3 shows an embodiment of a current mirror stage 14 according to the invention. The current mirror circuit includes a current input terminal 14A, a current output terminal 14B and a common terminal 14C. The input terminal 14A is connected to a photodiode A, which is represented here in the form of a signal current source Sph and a parasitic capacitance Cph. The output terminal 14B is connected to a load Zi2. A first controllable semiconductor element T1 is arranged between the current input terminal 14A and the common terminal 14C. A second controllable semiconductor element T2 is arranged between the current output terminal 14B and the common terminal 14C. In casu the semiconductor elements T1, T2 are connected to the common terminal via degeneration resistors R2, R3. The controllable semiconductor elements T1, T2 have interconnected control electrodes T1A, T2A which are also coupled to a bias voltage source V_{BIAS}, for biasing said control electrodes at a reference voltage.

The circuit further includes a transconductance stage 12 having an input 12A coupled to the current input terminal 14A and an output 12B coupled to the common terminal14C.

The circuit according to the invention is characterized in that the interconnected control electrodes T1A, T2A are coupled to the common terminal via a third controllable semiconductor element T3, and in that the bias voltage source V_{BIAS} is coupled to these control electrodes T1A, T2A via a control electrode T3A of the third controllable semiconductor element T3. The interconnected control electrodes T1A, T2A are further connected to a current source SI.

In the embodiment shown the transconductance stage 12 comprises a fifth controllable semiconductor element T5 which is arranged between its output 12B and ground GND. The fifth controllable semiconductor element T5 has a control electrode which is coupled to a common node 12D of a series arrangement of a further controllable semiconductor element M0 and a resistive impedance R1. The current source SI both biases the third and the fifth controllable semiconductor elements T3 and T5.

The circuit shown in Figure 3 operates as follows. If the photodiode provides an current Iph to the input terminal 14A of the current mirror, the transconductance stage 12 will withdraw a current Ic from the common terminal 14C of the current mirror such that the current Ii1 via the input terminal 14A equals the current Iph provided by the photodiode A. The operation of the current mirror formed by T1 and T2 has the effect that a current Io1 is delivered by the second controllable semiconductor element T2. The currents have a ratio Io1:Ii1 = P, P being the area ratio of the controllable semiconductor elements T1, T2. At the same time the control electrodes T1A, T2A of the controllable semiconductor elements T1, T2 respectively conduct a current Ib1, Ib2 such that $Ii1 = \alpha Ib1$ and $Io1 = \alpha Ib2$. As the third controllable semiconductor element T3 is biased by a current source, the signal currents Ib1+Ib2 will be conducted substantially from the common terminal 12B via the main current path of that semiconductor element T3. Hence these signal currents Ib1, Ib2 substantially do not contribute to the current Ic withdrawn by the transconductance stage 12. The current Ic therefore is Ii1(1+P). If the transconductance stage has an amplification gm, then the input resistance amounts

(1+P)/gm which is independent of the current amplification of the controllable semiconductor elements T1, T2.

In the known circuit which does not include a controllable semiconductor element T3 as in the invention, the input resistance amounts

$(1+P)(1+1/\alpha)gm$

Hence in the known circuit the input resistance is dependent on the amplification α of the controllable semiconductor elements. This is on its turn dependent on the current conducted by these elements. At low input currents the amplification α decreases, as a result of which the input resistance increases. This causes increasing signal losses at higher frequencies. In the circuit of the invention this phenomenon has been substantially annihilated.

Figure 4 shows a second embodiment of the current mirror according to the invention. In Figure 4 elements which have the same references are the same. This embodiment is characterized in that the first and the second semiconductor elements T1, T2 are bridged by a first and a second capacitive impedance C1, C2 having a capacitive value with a ratio of 1 to P. The first and the second capacitive impedances C1, C2 will respectively conduct signal currents Ic1 and Ic2, having a ratio Ic2/Ic1 = P. Hence the capacitive impedances C1, C2 contribute to the currents passing via the input and the output terminal 14A, 14B in the same ratio as the controllable semiconductor elements. As the frequencie of the input signal of the current mirror increases and the amplification factors of the controllable semiconductor elements T1, T2 decreases the capacitive impedances C1, C2 gradually take over the function of the semiconductor elements T1, T2.

Figure 5 shows a third embodiment of the current mirror according to the invention. Parts of Figure 5 having the same reference number as in Figure 4 are identical. The embodiment shown is characterized in that the interconnected control electrodes T1A, T2A are further connected via a third capacitive impedance C3 and via a fourth controllable semiconductor element T4 to a reference voltage GND. A control electrode T4A of the fourth controllable semiconductor element T4 is coupled to the common terminal 14C.

As illustrated in Figure 5, losses Ip may be caused by parasitic impedance Cp. However, as in this embodiment of the invention the parasitairy capacitor Cp, the bias voltage source, the base emitter transition of T3, the capacitive impedance C and the emitter base transition of T4 form a closed loop the sum of the voltages should be 0. From this it follows that the parasitic current Ip is completely compensated provided that the capacitance C3 is choosen equal to the parasitic capacitance Cp.

Figure 6 schematically shows an arrangement for reproducing an optical record carrier 30. The arrangement comprises a read head 40 including a radiation source 41 for generating a radiation beam 42. The read head further comprises an optical system 43 for directing the beam after interaction with the record carrier 30 to one or more photodiodes.

The read head 40 also comprises a signal processing circuit with respective amplifiers comprising a current mirror circuit according to the invention, for example according to one of the embodiments shown in Figures 3, 4 and 5. The current mirror circuits each have an input coupled to one of the photodiodes. In the embodiment shown the photodiodes and the amplifiers are together integrated at an IC 45 as shown schematically in Figure 1. A signal output of the signal processing circuit is coupled to a channel decoding circuit and/or an error correction circuit 50 for reconstructing an information stream Sinfo from the signal Sout provided by the signal processing circuit. The arrangement is provided with means 61, 62 for providing a relative movement between the read head 40 and the record carrier 30. In the embodiment shown the means 61 rotate the record carrier and the means 62 provide for a radial movement of the read head. Otherwise the means 61, 62 may for example be linear motors for moving the read head 40 and the record carrier respectively in mutually orthogonal directions.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. In the embodiments mainly bipolar transistors are shown. However, instead of bipolar transistors unipolar or MOSFET transistors can be used. In that case gate, source and drain of the unipolar transistor substitute respectively the base, emitter and collector, of the bipolar transistor. Multiple outputs are possible by providing copies of the transistor T2 between the common terminal 14C and additional output terminals 14B. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in a claim. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed general purpose processor. The invention resides in each new feature or combination of features.

CLAIMS.

1. Current mirror circuit including a current input terminal, a current output terminal and a common terminal, a first controllable semiconductor element arranged between the current input terminal and the common terminal, a second controllable semiconductor element arranged between the current output terminal and the common terminal, the controllable semiconductor elements having interconnected control electrodes which are also coupled to a bias voltage source, for biasing said control electrodes at a reference voltage, the circuit further including a transconductance stage having an input coupled to the current input terminal and an output coupled to the common terminal, characterized in that the control electrodes are coupled to the common terminal via a third controllable semiconductor element, and in that the bias voltage source is coupled to the control electrodes of the first and the second controllable semiconductor element via a control electrode of the third controllable semiconductor element.

2. Current mirror circuit according to claim 1, characterized in that, the interconnected control electrodes are further connected to a current source.

3. Current mirror circuit according to claim 1 or 2, characterized in that the first and the second semiconductor elements have an area ratio 1:P.

4. Current mirror circuit according to claim 3, characterized in that the first and the second semiconductor elements are bridged by a first and a second capacitive impedances having a capacitive value with a ratio of 1 to P.

5. Current mirror circuit according to claim 1, characterized in that the interconnected control electrodes are further connected via a third capacitive impedance and via a fourth controllable semiconductor element to a reference voltage, and that a control electrode of the fourth controllable semiconductor element is coupled to the common terminal.

6. Integrated circuit comprising at least one a current mirror circuit according to one of the claims 1 to 5, and a photodiode having an output coupled to its current input terminal.

7. Arrangement for reproducing an optical record carrier, comprising

a read head including a radiation source for generating a radiation beam, an optical system for directing the beam after interaction with the record carrier to one or more photodiodes,

respective amplifiers comprising a current mirror circuit according to one of the claims 1 to 5, each having an input coupled to one of the photodiodes,

a channel decoding circuit and/or an error correction circuit for reconstructing an information stream from the signal provided by an amplifier,

means for providing a relative movement between the read head and the record carrier.

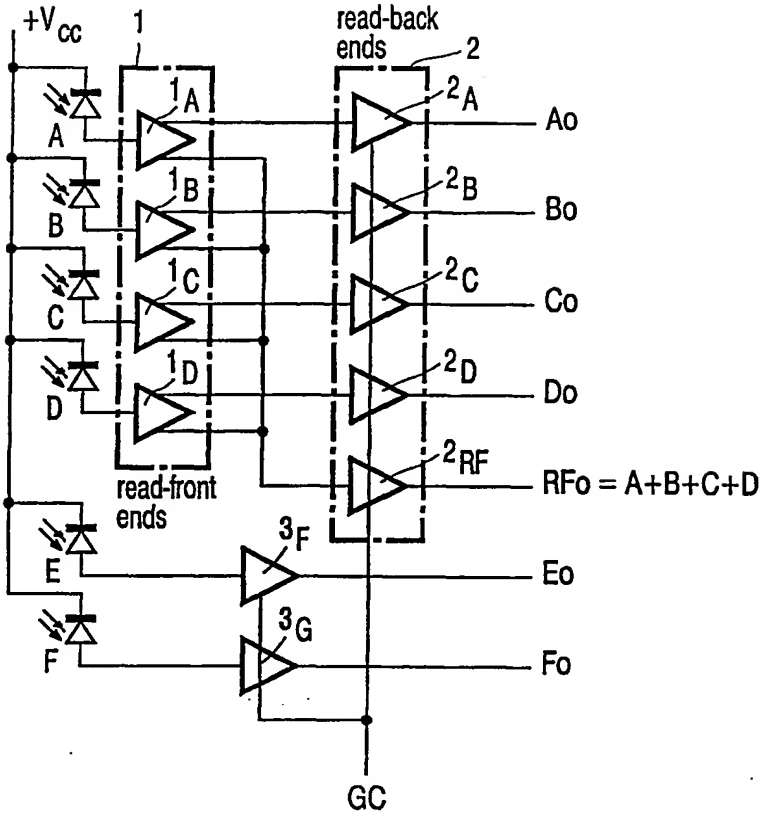

+Vcc
1
read-back ends
2
1A
2A
A
Ao
1B
2B
B
Bo
1C
2C
C
Co
1D
2D
D
Do
2RF
RFo = A+B+C+D
read-front ends
3F
E
Eo
3G
F
Fo
GC

FIG. 1

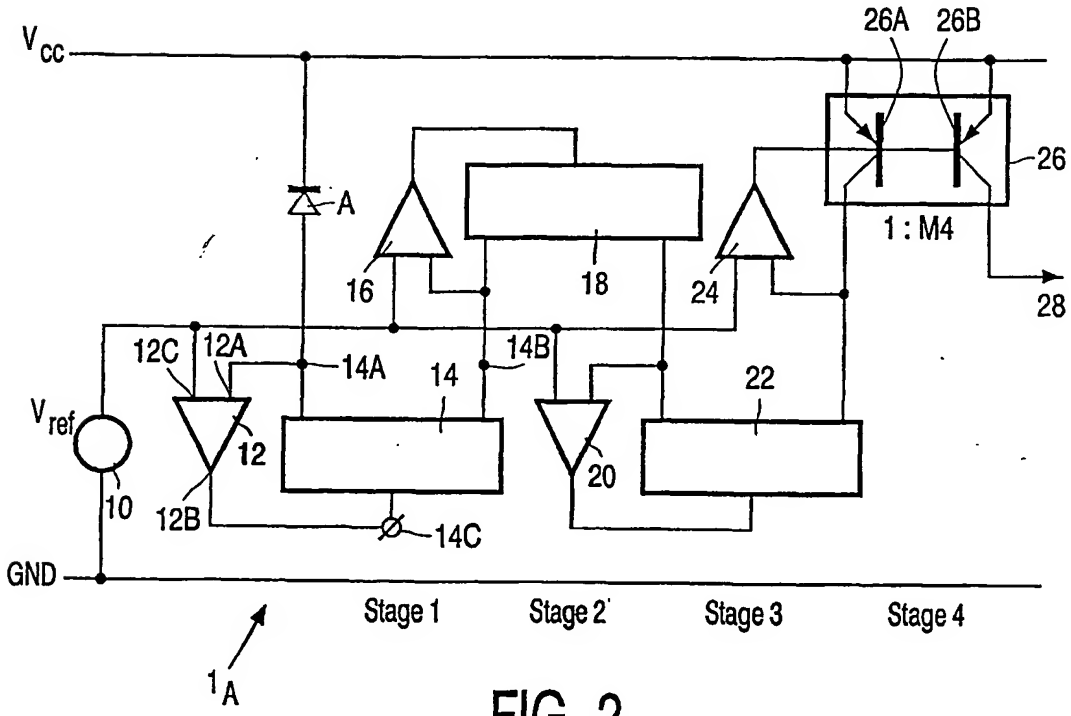

Vcc
26A
26B
26
A
1 : M4
16
18
24
28
12C
12A
14A
14
14B
22
Vref
12
20
10
12B
14C
GND
Stage 1
Stage 2
Stage 3
Stage 4
1A

FIG. 2

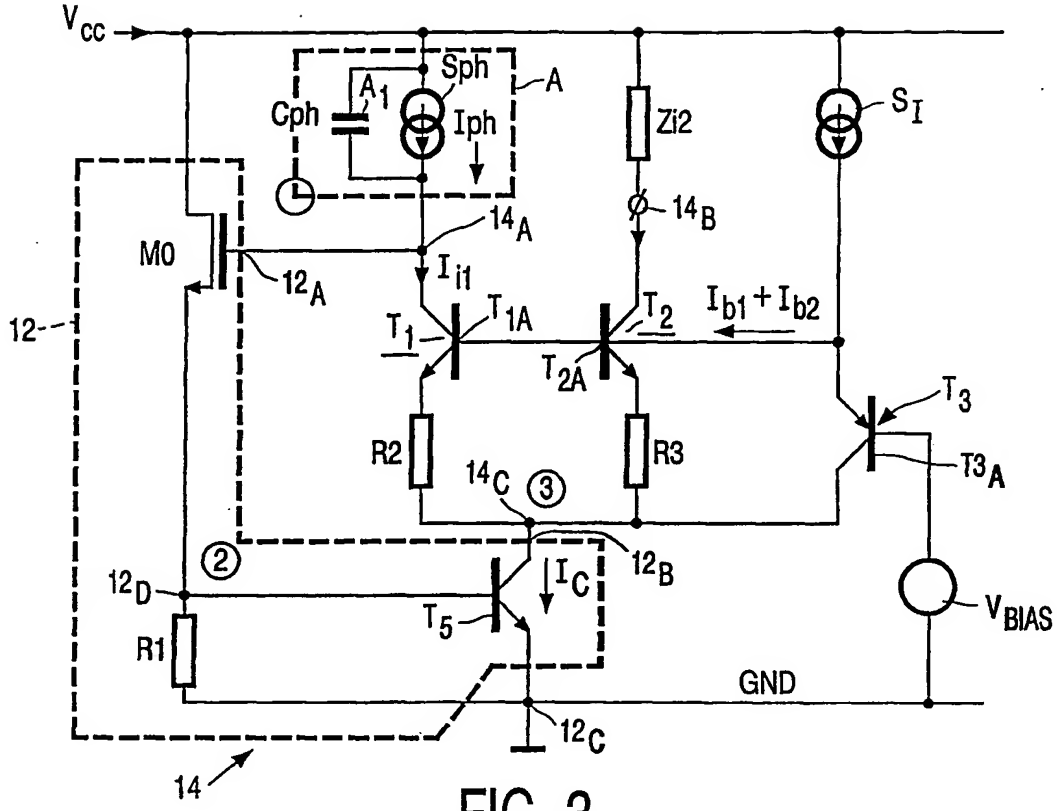

Vcc
Sph
A
A1
Cph
Iph
Zi2
SI
14B
14A
M0
12A
Ii1
12
T1
T1A
T2
Ib1+Ib2
T2A
T3
R2
R3
T3A
14C
3
2
12B
IC
12D
T5
VBIAS
R1
GND
12C
14

FIG. 3

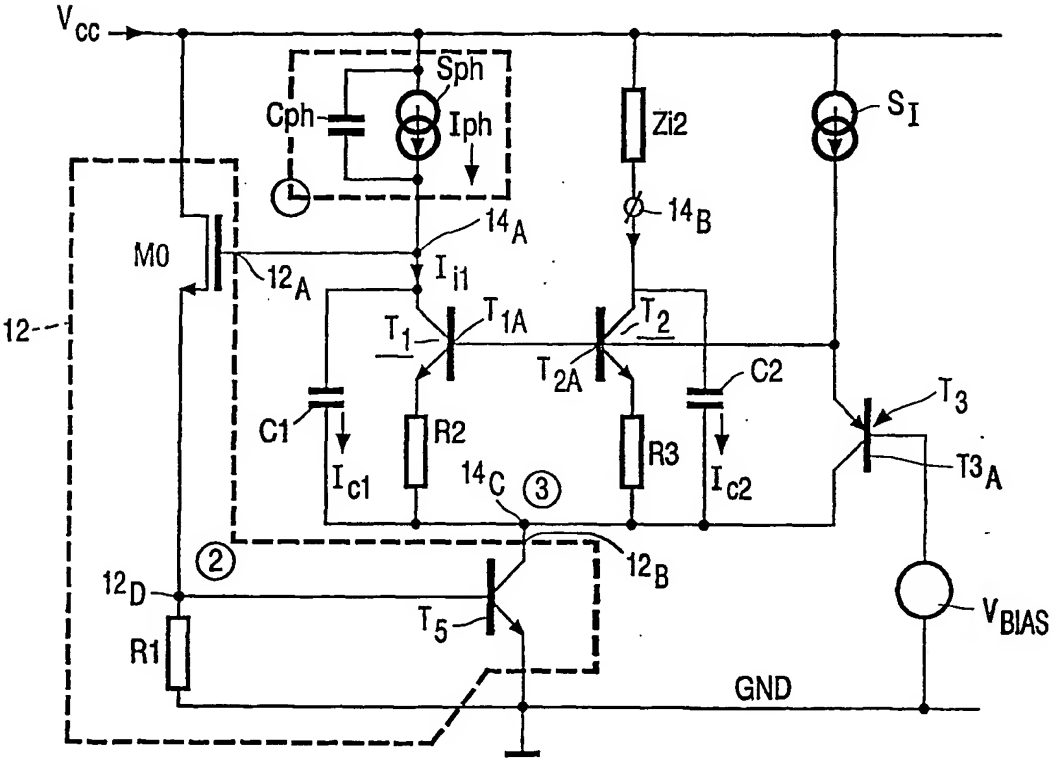

Vcc
Sph
Cph
Iph
Zi2
SI
14B
14A
M0
12A
Ii1
12
T1
T1A
T2
T2A
C2
T3
C1
R2
R3
Ic1
Ic2
T3A
14C
3
2
12B
12D
T5
VBIAS
R1
GND

FIG. 4

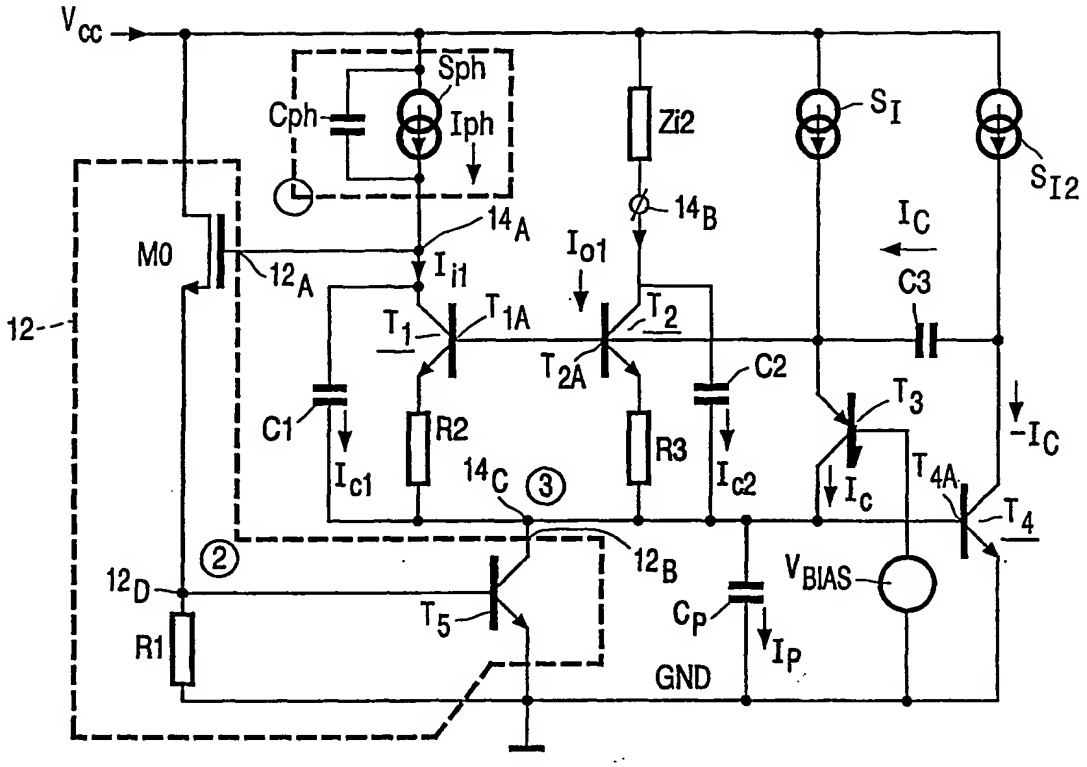

Vcc
Sph
Cph
Iph
Zi2
SI
SI2
14A
14B
IC
M0
12A
Ii1
Io1
C3
12
T1
T1A
T2
T2A
C2
T3
C1
R2
R3
-IC
Ic1
14C
3
Ic2
Ic
T4A
T4
2
12B
12D
VBIAS
T5
CP
R1
IP
GND

FIG. 5

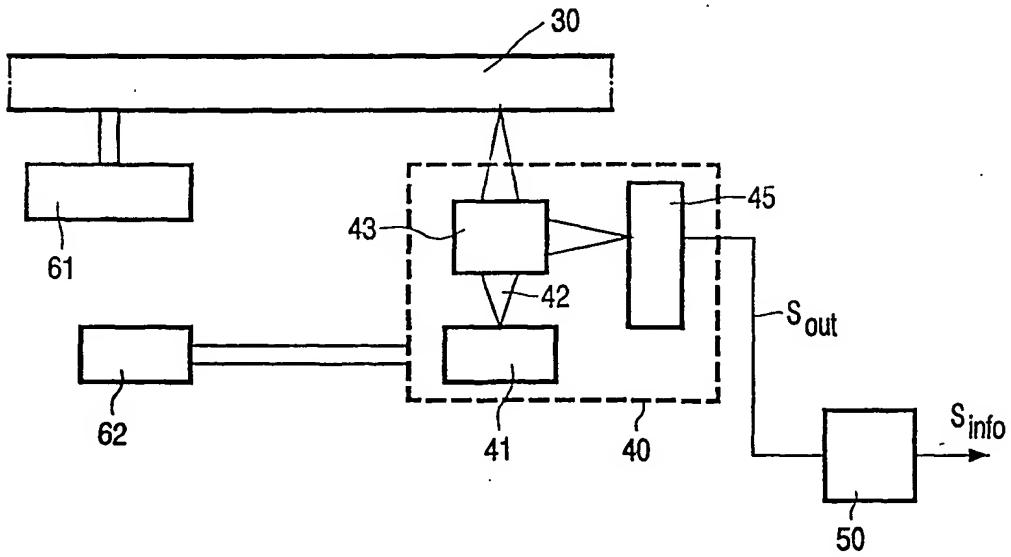

30
61
43
45
42
Sout
62
41
40
Sinfo
50

FIG. 6

INTERNATIONAL SEARCH REPORT

Ir ...nal Application No
PCT/EP 01/10110

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G05F3/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G05F H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 00 31604 A (KONINKL PHILIPS ELECTRONICS NV) 2 June 2000 (2000-06-02) cited in the application the whole document	1-7
A	US 4 769 619 A (TAYLOR STEWART S) 6 September 1988 (1988-09-06) the whole document	1-7
A	US 5 337 021 A (ZARABADI SEYED R ET AL) 9 August 1994 (1994-08-09) the whole document	1-7

[ ] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 January 2002	18/01/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Schobert, D

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Ir nal Application No
PCT/EP 01/10110

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 0031604 A	02-06-2000	WO 0031604 A1	02-06-2000
		EP 1057091 A1	06-12-2000
		US 6323723 B1	27-11-2001
		US 2001038301 A1	08-11-2001
US 4769619 A	06-09-1988	EP 0257345 A2	02-03-1988
		JP 1829352 C	15-03-1994
		JP 63054006 A	08-03-1988
US 5337021 A	09-08-1994	NONE	

INTERNATIONAL SEARCH REPORT

IB2004/051986

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F3/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 387 951 A (PHILIPS NV) 19 September 1990 (1990-09-19) column 7, line 1 - line 20; figure 2	1,2,4,8
X	US 4 728 815 A (MAIN W ERIC) 1 March 1988 (1988-03-01) abstract; figure 4	1,2,4,8
A	US 2002/180490 A1 (VOORMAN JOHANNES OTTO ET AL) 5 December 2002 (2002-12-05) cited in the application the whole document	1-9
A	US 2001/038301 A1 (FRAMBACH JOHANNES P A ET AL) 8 November 2001 (2001-11-08) figures 3-6	1-9

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 December 2004	27/01/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Kurzbauer, W

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

IB2004/051986

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 399 991 A (MORAVEJI FARHOOD) 21 March 1995 (1995-03-21) figures 2,3A	1,9

INTERNATIONAL SEARCH REPORT

IB2004/051986

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0387951 A	19-09-1990	DE 69011366 D1	15-09-1994
		DE 69011366 T2	23-02-1995
		EP 0387951 A1	19-09-1990
		HK 44296 A	22-03-1996
		JP 2274109 A	08-11-1990
		JP 2869664 B2	10-03-1999
		KR 149650 B1	01-09-1999
		US 5038114 A	06-08-1991
US 4728815 A	01-03-1988	GB 2196499 A ,B	27-04-1988
		JP 2082615 C	23-08-1996
		JP 7105698 B	13-11-1995
		JP 63114410 A	19-05-1988
		KR 9507691 B1	14-07-1995
US 2002180490 A1	05-12-2002	CN 1388924 T	01-01-2003
		WO 0219050 A1	07-03-2002
		EP 1316005 A1	04-06-2003
		JP 2004507955 T	11-03-2004
US 2001038301 A1	08-11-2001	WO 0031604 A1	02-06-2000
		EP 1057091 A1	06-12-2000
		JP 2002530971 T	17-09-2002
		US 6323723 B1	27-11-2001
US 5399991 A	21-03-1995	NONE	